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## Where analog really meets digital

[Stephan Ohr](#)[EE Times](#)

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One of my favorite superheroes when I was a kid was a red-suited runner called The Flash. This guy could run so fast that he could make time stand still, accomplishing many different tasks within incredibly short intervals-like one beat of a human heart, or one tick of a second hand on the face of a clock.

Although the electronics industry is not quite as anthropomorphic, it has its own version of The Flash. Clocks and timing generators have the ability to take finer slices of electronic states. In doing so, they serve as the true interface between analog and digital segments.

I explained in a previous column how ever-finer time slicing-and oversampling in particular-lends itself to higher-resolution A/D conversion. Instead of forcing the data converter to make fine gradations on a rapidly changing signal amplitude, digital oversampling tends to flatten those signal peaks and valleys. Thus, the delta-sigma data converter only cares whether the signal is rising or falling within a given time segment. If you raise the sampling rate high enough, the differences in amplitude from sample to sample become almost undetectable.

The truth is that interface components like data converters, communications backplane transceivers and serial data buses all depend on increasingly fast and precise clocking. This is no longer a specialty of digital systems houses like Freescale, Integrated Device Technology (IDT) or Cypress Semiconductor, but is in fact spilling over into analog realms.

Analog houses like Analog Devices, Texas Instruments and Maxim Integrated Products, and even Micrel Semiconductor, are expanding their portfolios of clock generators and timing circuits. These vendors are beefing up their offerings in hopes of capturing a share of the roughly \$1 billion clock generator total available market, which was dominated by Integrated Circuit Systems (ICS) until its recent purchase by IDT. But they're also expanding in this area because precise waveform control-the drumbeat for the entire digital system-is increasingly an analog talent.

Coincidentally, ADI's entry into the clock generator realm actually follows Lattice Semiconductor's. The parts are very similar and attention-getting in what they propose to do: generate multiple in-system clock signals. Their outputs are programmable, allowing designers to compensate for timing skews and wiring path delays that can show up on the surface of a pc board.

Lattice's ispClock5500 programmable clock generator family includes a 10-

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output device (the 5510) and a 20-output device (the 5520). Users can select up to five clock frequencies ranging from 10 MHz to 320 MHz, each with programmable skew control. ADI's clock distribution ICs (the AD951x family) offer a smaller number of outputs (up to eight) but use a 6 bit (with 64 increments) to control the delay settings on each line from 1 to 10 nanoseconds. Low-voltage positive emitter-coupled logic, LVDS and LVCMOS are the favored interfaces for these and other manufacturers' parts.

Jitter control, the care-about for anything that proposes precision timing within the space of a human heartbeat, is on the order of a few picoseconds (250 femtoseconds rms for Analog Devices' part).

Once you've internalized that, expect to see the words "low jitter" on every data sheet you pick up. Maxim's MAX9492, for example, provides "six low-jitter outputs," one of which is the buffered output of the reference clock. The other five outputs are independently programmable to generate all clock frequencies typically required in a network or storage line card: 133, 125, 83, 66, 62.5, 50, 33 and 25 MHz. Output-to-output skew is rated at 220 ps, and the output jitter control is said to be less than 10 ps.

Texas Instruments' recently introduced CDCM7005 is promoted as "a clock synthesizer and jitter cleaner" with low phase noise (-138 dB down at many output frequencies). The synthesizer includes a built-in 2.2-GHz voltage-controlled oscillator and is targeted at 2.5G/3G wireless basestations and other data communications applications, as well as medical imaging and test and measurement. You have to hunt for its jitter figure on the data sheet, though: It varies with frequency. (We can make a beefy planetanalog.com technical article on just the test circuits shown on this data sheet.) Jitter is roughly 282 fs for an LVPECL line outputting a 61.44-MHz pulse, and 230 fs for LVCMOS.

Micrel, whose talent base includes low-dropout regulators and power-management devices, recently issued a clock generator, the SY89840U, that suppresses runt pulses. A not-particularly-fast part, its random jitter spec is less than 1 ps rms. Its promotional materials say it is targeted at switching architectures in enterprise servers and non-Sonet-based networking systems.

With a broad portfolio of clock generators and synthesizers, Cypress Semiconductor offers clocks that generate, modify, buffer or distribute a pulse. If you're interested, Cypress has a good tutorial on planetanalog.com, "A Planet Analog Primer: A Clock For Every Timing Need." Search article ID: 163702482.

In most systems, the clock generator does not interface with the communications line or provide direct timing for the system CPU. (There are multiplier and divider circuits that can slice a pulse into finer steps.) Consequently, Maxim's clocks fit a wide variety of applications just by putting out 200-MHz pulses.

Exar's multipulse generators, the XRK7933, XRK7955 and XRK7988, go up to 400 MHz. The fastest clocks from ICS appear to output pulses in the 700-MHz range, depending on the interface. ADI's multi-output part puts out 800 MHz on its LVDS lines and 250 MHz on its CMOS lines, though they'll take in 1.5-GHz inputs. The specs for Texas Instruments' CDCM7005-the only one mentioned here that targets RF-says it will output pulses as high as 1.5 GHz.

It may be a while before we see a programmable multi-output clock generator that spits out a full set of gigahertz pulses for non-RF clocking systems. But this ability to go within time periods would support setup-and-hold time requirements not just for data converters but also for digital ASICs, FPGAs, digital up/down converters and all sorts of divider circuits.

Just what is a digital clock, after all? Remember that something as seemingly

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complex as a Pentium processor is in fact a Rube Goldberg contraption, driven at its source by a monkey jerking a pump handle up and down. But imagine how much work could be accomplished if that monkey jerked the pump handle several billion times a second.

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