

## 6-pin, 8-bit Microcontroller



Get what you need to get started now.  
Click here to get a demo board, samples and code.



## SEARCH THIS SECTION

WHAT'S NEW REVIEWS BRIEFS FOCUS ON OPINION DATA SHEETS NETSEMINARS PRESS RELEASES

## Newcomer unveils zero delay buffers

Bettyann Liotta

eeProductCenter

(09/27/2005 11:34 AM ET)

E-MAIL PRINT



SEARCH DATA SHEETS

EETIMES'



## PRODUCT CATEGORIES

ANALOG ICs

BOARDS / BUSES

DSP

ELECTROMECHANICAL

EMBEDDED TOOLS

INTERCONNECTS

MPUS / MCUS

MEMORY

LOGIC &amp; INTERFACES

PASSIVES / SENSORS

PLDS / FPGAs

POWER COMPONENTS

POWER SOURCES

RF / MICROWAVE

TEST / MEASUREMENT

SEARCH

## "The Manufacturer Says:"

Fremont, Calif. — Exar Corp. kicked off a new family of zero delay buffers with two devices that tout low-skew and low-noise capabilities at 3.3 V.

The XRK32510 and XRK39910 are said to be cost-effective zero delay buffers (ZDBs) for a wide range of applications spanning from consumer and industrial to networking and computing.

"This marks Exar's fourth clock and timing introduction and reaffirms Exar's focus on not only this market but the company's ongoing commitment to delivering customers a wide range of device options," said Bahram Ghaderi, vice president and general manager, network and transmission products division. "Leveraging our extensive analog and phase-locked loop (PLL) design expertise, we have extended this product line to include more features and functionality for customers' clock distribution needs."

Exar previously introduced intelligent dynamic clock switch (IDCS) devices and a portfolio of 3.3-V programmable skew buffers (PSBs).

[Click here for more details on Exar's IDCS devices at eeProductCenter.](#)

Operating at speeds up to 175 MHz, the ZDB clock drivers are designed for use with synchronous dynamic random access memory modules found in computing systems, plus telecommunications and networking applications. The devices accurately align the feedback output to the clock input signal ensuring a zero delay through the IC. Each device distributes one clock input to a bank of ten outputs, resulting in low-skew, low-jitter copies of each clock, Ghaderi said. "The family offers tight peak-to-peak jitter spec at less than 75 picoseconds to ensure the production of stable and clean signals," he said.

The XRK39910 is a fanout PLL clock driver intended for high performance computing and data-communications

## "eeProductCenter's Bettyann Liotta Says:"

What makes Exar think that they can go up against established giants in the ZDB market like Cypress Semiconductor Corp., Freescale Semiconductor Inc., and Integrated Circuit Systems Inc.?

"We use newer technology processes (.35 micron CMOS) and offer more advantages in terms of cost and performance," said John Demiray, Exar's senior director of product marketing, network and transmission products.

Although this is Exar's first crack at ZDBs, Demiray believes that Exar's experience with PLL technology, combined with low priced products and some integrated features that aren't currently available in competing ZDBs, will enable the company to grab a hunk of the pie.

Exar's IDCS and PSB clock products utilize PLL technology as well. "The core technology is the same for these devices but the end applications are different," Demiray said.

Exar's IDCS and PSB devices are mainly focused on the communications sector. These new lower priced ZDBs will enable the company to gain entry into the consumer market, Demiray said.

Designers want to be able to take a single output and generate multiple copies of the output, Demiray said. The XRK32510 ZDB has 10 outputs based on a single input. "Therefore, you can have a single source and generate 10 copies of the clock on a PC board since all of the components are utilizing the same clock," he said. (*See Clock Board Overview slide below*)



[See Clock Board Overview Slide](#)

In addition to making standard size parts that can be used interchangeably, Exar has added some unique integrated features to its first ZDBs,



## WEB SITES

AUDIO DESIGNLINE

AUTOMOTIVE DESIGNLINE

DIGITAL TV DESIGNLINE

DSP DESIGNLINE

GREEN SUPPLYLINE

INDUSTRIAL CONTROL DESIGNLINE

MOBILE HANDSET DESIGNLINE

NETWORK SYSTEMS DESIGNLINE

POWER MANAGEMENT DESIGNLINE

PROGRAMMABLE LOGIC DESIGNLINE

VIDEO/IMAGING DESIGNLINE

WIRELESSNET DESIGNLINE

EETIMES

COMMSDESIGN

EEDESIGN

EMBEDDED.COM

PLANET ANALOG

SILICON STRATEGIES

ELECTRONIC SUPPLY AND MANUFACTURING

NETSEMINAR

## SITE FEATURES

PRODUCT SHOPPER

NEW PRODUCT INFO

SPEC SEARCH

applications. The internal loop filter is tuned to minimize the jitter (or frequency variation), while still providing accurate responses to input frequency changes. The XRK39910 offers eight zero delay outputs with less than 250 ps of output-to-output skew, selectable positive or negative edge synchronization, output frequency of 15 MHz to 85 MHz, and low jitter of less than 200 ps peak-to-peak.



[See related diagram](#)

The XRK32510 is available now in a 24-pin TSSOP for \$2.20 each in 10,000-unit quantities. [Click here for the XRK32510 data sheet](#). The XRK39910, which sells for \$1.95 in like quantities, will be available in a month in a 24-pin SOIC package. [Click here for the XRK39910 data sheet](#).

**Exar**, 1-510-668-7000, [www.Exar.com](http://www.Exar.com).

Demiray said. "Sometimes external circuitry is needed to change the impedance on a board. We are now adding that capability," he explained. In some instances, resistors or level translators are required to achieve the same functionality. While resistors typically cost only pennies, the ICs can cost as much as .50 cents to \$1.00 each per output. "Consequently, 10 outputs can add a significant amount to the cost of the ZDB," Demiray said.

The ZDBs also tout low skew. "At 250 ps, these buffers offer of the lowest slew rates in the industry," Demiray said.

In July, Alliance Semiconductor Corp. (Santa Clara, Calif.) expanded its product offering with a new family of ZDB's and non-zero delay buffers (NZDB's).

The ASM5000 family of PLL-based ZDB's and the ASM2000 family of non-PLL-based NZDB's were designed to address the clocking needs (greater than 250 MHz) of various data communications, networking, telecommunications, industrial and many consumer systems.

[Click here for a closer look at Alliance's ZBD and NZDB devices at eeProductCenter.](#)

## Related Stories:

- » [Clocking requirements spur buffer demand](#)
- » [Clock devices target mission critical applications](#)

## Electronic Marketplace

### [The Premier Publication for EE Designers](#)

Learn about the latest EDA industry trends and newest must-have products in the EDA Tech Forum Journal, a free, quarterly publication of technical articles written by your EE design peers, industry analysts and EDA solution providers. Subscribe now!

### [Intel Communications Alliance](#)

Connect with world class community of communications and embedded developers. Quickly locate products and solutions that can help speed development cycles and cut costs.

### [Single-chip ADC + Precision Digital Filtering](#)

The QF4A512 combines 4 channels of Analog Signal Conditioning, 16-bit ADC and Precision, Programmable Digital Filters in a single chip. Quickfilter Pro software and Development Kit configures and verifies your application in just minutes.

### [Locate hard to find Electronic Parts](#)

Specializes in locating obsolete or short supply electronic parts and components. Visit our website today and do a free part search.

### [Free Webinar! GHz Board Design Signal Integrity](#)

Learn for GHz designs: relevant interconnect standards, BER prediction and analysis, signal integrity performance factors, via and power plane design, NRZ and 4PAM signaling differences, 8B10B encoding benefits, eye diagram analysis. Free webinar.

[Click here to get your listing up.](#)

All material on this site [Copyright © 2006 CMP Media LLC](#). All rights reserved.  
[Privacy Statement](#) | [Your California Privacy Rights](#) | [Terms of Service](#).