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## Clock buffers blow away competition?

[Bettyann Liotta](#)
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San Jose, Calif. — Cypress Semiconductor Corp. released zero-delay buffers (ZDBs) that are said to outperform all pin-compatible products for high-speed communications and consumer devices in terms of operating frequency and cycle-to-cycle jitter.

The CY23EP05 and CY23EP09 phase-locked loop (PLL) clock buffers offer the highest operating frequency, the lowest cycle-to-cycle jitter and the lowest output-to-output skew on the market, said Wendy Zhou, marketing manager for Cypress's timing distribution products. The products add to Cypress's portfolio of timing solutions for applications such as multi service routers and switches, basestations, plasma displays and set-top boxes.

Cypress's enhanced performance ZDBs offer 220-MHz maximum operating frequency and 3.3- or 2.5-V operating voltage. In addition, the CY23EP05 and CY23EP09 offer best-in-class performance with 55-ps cycle-to-cycle jitter and 100-ps output-to-output skew, Zhou said. Both ZDBs are available in lead-free packages.

Last month, Exar Corp. (Fremont, Calif.) threw its hat in the ZDB ring with two buffers touting low-skew and low-noise capabilities at 3.3 V.

[Click here for more details on Exar's ZDBs at eeProductCenter.](#)

Alliance Semiconductor Corp. (Santa Clara, Calif.) also recently introduced a new family of ZDB's that were made to address clocking needs greater than 250 MHz.

[Click here for more details on Alliance's ZDBs at eeProductCenter.](#)

Cypress' 5-output CY23EP05 is offered in an 8-pin, SOIC package for 75 cents each in 1,000 unit quantities. [Click here for the CY23EP05 data sheet](#)

The 9-output CY23EP09 is offered in a 16-pin, SOIC or a TSSOP. It is priced at \$1.10 each in same quantities. [Click here for the CY23EP09 data sheet.](#)

**Cypress Semiconductor Inc.**, 1-408-943-2600, [www.Cypress.com](http://www.Cypress.com). (See Cypress block diagram below).

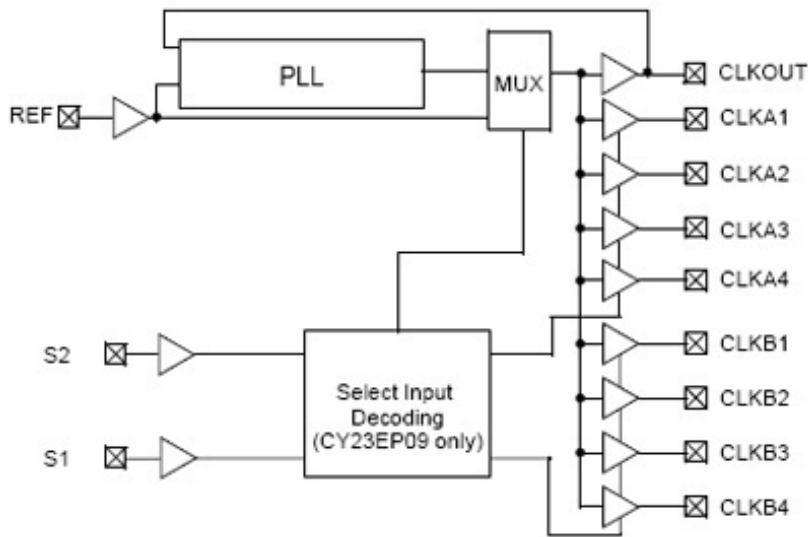
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## Block Diagram



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