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## Clock Generation Gets Redundancy And Reduced Skew

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ED Online ID #10225

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As clock speeds increase with each generation, it gets tougher to produce a clean clock that can be distributed with minimum skew to multiple circuits. But Exar's Intelligent Dynamic Clock Switch (IDCS) line of clock-driver ICs makes clock generation easy.

These ICs take a clock oscillator input and generate multiple clock outputs with minimum skew and redundancy. The XRK-7933 has a 33.3- to 100-MHz output and targets computing applications. The XRK7955 has an output range of 25 to 125 MHz and fits 10/100 Ethernet products. The XRK7988 has a 19.44- to 155.52-MHz output and fits Sonet/SDH products at the OC-3 level.

The clock drivers accept two low-voltage PECL (LVPECL) differential clock inputs and generate five LVPECL differential outputs. Two of the outputs regenerate the input signal for phase and frequency, while the other three outputs generate 3x (XRK7933), 5x (XRK7955), or 8x (XRK7988) signals that are phase-aligned. The outputs are derived from the internal phase-locked loop and output dividers.

The dynamic clock switch (DCS) circuit continuously monitors both input clocks. If the primary clock fails, the DCS switches to the secondary clock, which completes the phase and frequency

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alignment with minimum output phase disturbance.

Samples are available now. The 1000-unit quantity price for each is \$8.75.

Exar Corp.  
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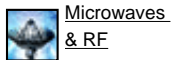
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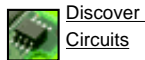
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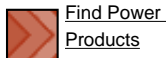
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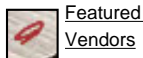
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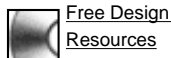
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